Small signal parameter extraction of GaAs and GaN devices

A Project Report
Submitted by

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Summer Internship Certificate

This is to certify that Mr./Ms. VARUN KUMAR M of NIT, KARNATAKA has participated in the ***Summer Internship Program*** under my guidance at the Centre for Nano Science and Engineering (CeNSE), Indian Institute of Science, Bangalore, during MAY - JULY 2019.

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Abstract

In this project, we implement a method to extract the small signal parameters of GaN and GaAs devices. This method consists in a direct determination of both the extrinsic and intrinsic small-signal parameters in a low frequency band. From, the extrinsic parameters and S parameters of the device, the intrinsic parameters are determined. This method is fast and accurate, and the determined equivalent circuit fits the S-parameters very well up to 26.5 GHz.

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Introduction

Knowledge of the small-circuit equivalent circuit of a field effect transistor is very useful for the device performance analysis (gain, noise, etc.) in designing of microwave circuits and characterizing the device technological process. Usually, the small-signal equivalent circuit is obtained by optimizing the component values to closely fit the small-signal microwave scattering parameters measured on the device.

1.1 Problem Definition

The main objective is to extract the intrinsic and extrinsic parameters of GaN HEMTs, ultimately obtaining the Y parameters of the intrinsic device. The required parameters are extracted through measurement of S parameters of the device and various bias conditions. The extrinsic parameters are first determined. The intrinsic parameters are determined with the help of the extrinsic parameters extracted initially.

1.2 Motivation

Usually, the small-signal equivalent circuit is obtained by optimizing the component values to closely fit the small-signal microwave scattering parameters measured on the device. However, this equivalent circuit determination has several drawbacks:

1. Accurate broad-band S-parameter measurement is required.
2. For small differences in the error function, the optimum element values can vary depending upon the optimization method and the starting values.
3. To have a physical significance, the equivalent circuit requires a preliminary determination of certain parameters (gate resistance or inductances,for example).

In order to overcome these difficulties we have chosen to implement the method as given in [2] to determine the FET small-signal equivalent circuit. This method consists in a direct, fast, and accurate measurement of the different elements performed at relatively low frequency.

Description

2.1 Theoretical Analysis

The conventional small-signal equivalent circuit of a field effect transistor is shown in Fig. 1. Basically, this equivalent circuit can be divided into two parts:

1. Since the intrinsic elements g_m, g_d, C_{gs}, C_{gd} (which includes,in fact, the drain-gate parasitic), $C_{ds}, R_i, and\tau$, which are functions of the biasing conditions;

2. the extrinsic elements $L_g, R_g, C_{pg}, L_s, R_s, R_d, C_{pd}, andL_d$, which are independent of the biasing conditions.

Since the intrinsic device exhibits a PI topology, it is convenient to use the admittance (Y) parameters to characterize its electrical properties. These parameters are:

$$\begin{aligned} y_{11} &= \frac{R_i C_{gs}^2 \omega^2}{D} + j\omega\left(\frac{C_{gs}}{D} + C_{gd}\right) \\ y_{12} &= -j\omega C_{gd} \\ y_{21} &= \frac{g_m \exp(-j\omega\tau)}{1+jR_i C_{gs}\omega} - j\omega C_{gd} \\ y_{22} &= g_d + j\omega\left(C_{ds} + C_{gd}\right) \end{aligned} \tag{2.1}$$

with $D = 1 + \omega^2 C_{gs}^2 R_i^2$
For a typical low-noise device, the term W'C R? is less than 0.01 at low frequency (F< 5 GHz) and D =1 constitutes a good approximation. In addition, assuming WT « 1, we have

$$\begin{aligned} y_{11} &= R_i C_{gs}^2 \omega^2 + j\omega\left(C_{gs} + C_{gd}\right) \\ y_{12} &= -j\omega C_{gd} \\ y_{21} &= g_m - j\omega\left(C_{gd} + g_m\left(R_i C_{gs} + \tau\right)\right) \\ y_{22} &= g_d + j\omega\left(C_{ds} + C_{gd}\right) \end{aligned} \tag{2.2}$$

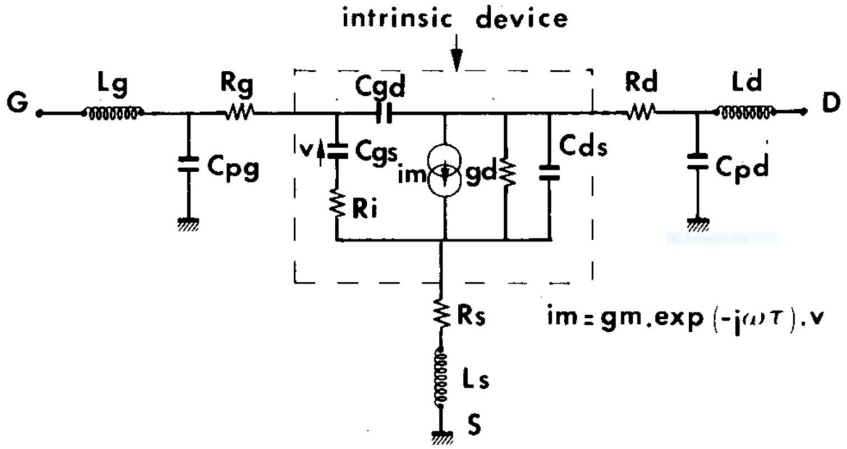


Figure 2.1: Small signal equivalent circuit of a field effect transistor

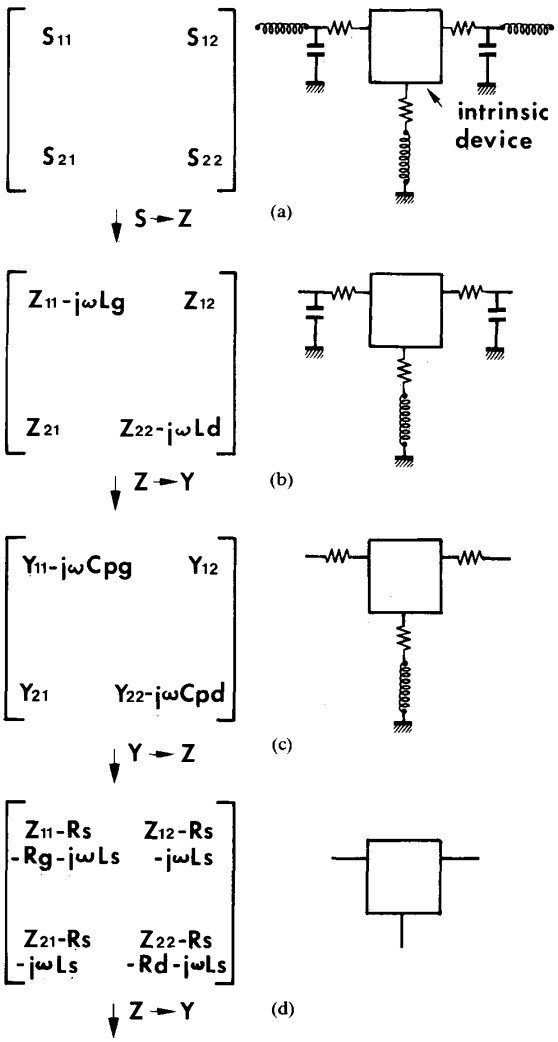


Figure 2.2: Method for extracting the device intrinsic Y matrix

2.2 Measurement of the equivalent circuit extrinsic elements

2.2.1 Determination of the Parasitic Resistances and Inductances

The S-parameter measurements at zero drain bias voltage can be used for the evaluation of device parasitics because the equivalent circuit is much simpler. In this project, all the parasitics are directly deduced from measurements performed at $V_{ds} = 0$.For any gate biasing conditions, the impedance parameters z_{ij} can be written:

$$\begin{aligned} z_{11} &= R_c/3 + z_{dy} \\ z_{12} &= Z_{21} = R_c/2\omega L_s \\ z_{22} &= R_c \end{aligned} \tag{2.3}$$

where R_c, is the channel resistance under the gate and z_{dy} is the equivalent impedance of the Schottky barrier. z_{dy} can be written

where n is the ideality factor, k the Boltzmann constant, T the temperature, C_g, the gate capacitance, and I_g, the dc gate current. As the gate current increases, R„ decreases and C, increases but the exponential behavior of R„ versus Vgs is the dominant factor; consequently the term Rdy. Cg. o tends to zero for gate current densities close to $5 * 10^7 - 10^8$ A/m2. In that case we have,

For such a gate current, the capacitive effect of the gate disappears and the z_{11} parameter becomes real:

In addition, the influence of the C_{pg} and Cpd, parasitic capacitances is negligible and consequently the extrinsic Z parameters are simply determined by adding the parasitic resistances R_s, R_g, R_d, and inductances L_g, L_s, L_d to the intrinsic Z parameters. Then we have

$$\begin{aligned} Z_{11} &= R_s + R_g + \tfrac{R_c}{3} + \tfrac{nkT}{qI_g} + j\omega\left(L_s + L_g\right) \\ Z_{12} &= Z_{21} = R_s + R_c/2 + j\omega L_s \\ Z_{22} &= R_s + R_d + R_c + j\omega\left(L_s + L_d\right) \end{aligned} \tag{2.4}$$

2.2.2 Measurement of the C_{pg} and C_{pd} Parasitic Capacitances

In the previous section it has been shown that suppressing the capacitive effect of the gate provides the series elements. Following the same philosophy, the input and output C_{pg}, and C_{pd} parasitic capacitances are measured by suppressing the conductivity of the channel. As a matter of fact, at zero drain bias and for a gate voltage lower than the pinchoff voltage 5, the intrinsic gate capacitance (i.e., under the gate) cancels, as

does the channel conductance.
For frequencies up to a few gigahertz, the resistances and inductances have no influence on the imaginary part of the Y parameters, which can be written:

$$\begin{aligned} \mathrm{Im}\,(Y_{11}) &= j\omega\,(C_{pg} + 2 \cdot C_b) \\ \mathrm{Im}\,(Y_{12}) &= \mathrm{Im}\,(Y_{21}) = -j\omega C_b \\ \mathrm{Im}\,(Y_{22}) &= j\omega\,(C_b + C_{pd}) \end{aligned} \tag{2.5}$$

where C_b, represents the fringing capacitance due to the depleted layer extension at each side of the gate.
These expressions show that the imaginary part of the 2 parameters increases linearly versus frequency while the real part is frequency independent. In addition it must be noted that the real part of Z_{11} increases as $1/I_g$.

Therefore the Z parameters' real parts provide three relations between the four unknowns R,, R_g, R_d, and R_c. At this step, an additional relation is needed to separate the four unknowns. This additional relation can be:

1. The value of the sum $R_s + R_d$, determined by the conventional method. It must be emphasized that this determination can be carried out with the network analyzer using the real part of Z_{22}.

2. The value of R, if it can be provided from the resistance measurement from pad to pad.

3. The value of R_s and R_d provided by dc measurements.

4. The value of R_c if the channel technological parameters are known.

In conclusion, the series parasitic elements R_s, R_g, R_d, L_s, L_g, and L_d can be provided by S-parameter measurement performed under zero drain bias and forward gate bias voltage condition.

Results

According to the mathematical equations developed in the previous section, the the extrinsic parameters of the device were estimated. The S parameters of the entire device were measured using a network analyser. From these, graphs corresponding to equations (2.4) and (2.5) were plotted. From the slopes of the graphs, the extrinsic capacitances and extrinsic inductances were obtained which was then used to calculate the instrinsic parameters according to figure 2.2 using matlab scripts in MATLAB 2019a.

3.1 Extrinsic Capacitances

The extrinsic capacitances were obtained by plotting the imaginary part of Y parameters with frequency. The slopes were used to determine the corresponding capacitances.

Device	Cb (fF)	Cpd (fF)	Cpg (fF)
R2282_VG-7_Vd0V_Id14nA	39.52146	34.66844	14.84673
R2282_A5,5_VG-7V_Vd0V_Id3nA	139.1116	49.15198	8.197802
R2282_A5,1_VG-7_Vd0V_Id3nA	109.8737	43.38970	13.62020
R2282_A4,1_VG-7_Vd0V_Id2nA	111.2421	43.30947	9.805376
R2282_A3,4_VG-7V_Vd0V_Id4nA	107.8583	44.91280	7.984918
R2282_A3,1_VG-7_Vd0V_Id5nA	111.2958	41.25522	11.91420
R2282_A2,3_VG-7_Vd0V_Id3nA	108.2490	38.14607	8.498910
R2282_A1,2_VG-7V_Vd0V_Id3nA	74.38542	38.27541	12.02635

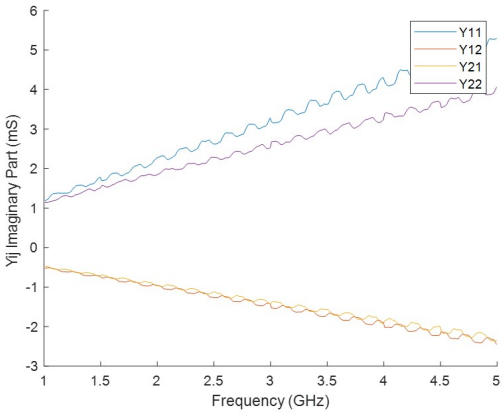
Table 3.1: Summary of extrinsic capacitances

3.2 Extrinsic Inductances

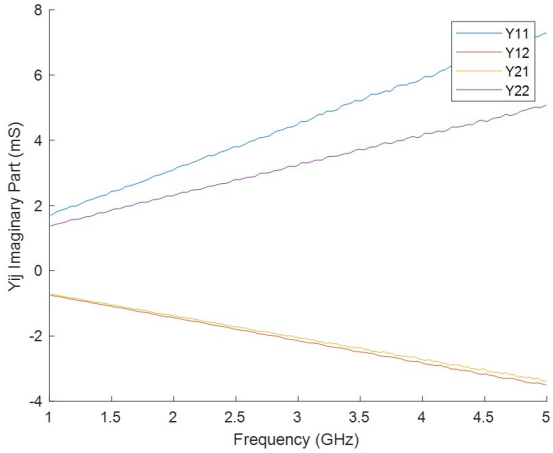
The extrinsic inductances were obtained by plotting the imaginary part of Z parameters with frequency. The slopes were used to determine the corresponding inductances.

Device	Ls (nH)	Ld (nH)	Lg (nH)
R2282_A1,1_VG1_Vd0V_Id140nA	0.468959	0.124437	20.2307
R2282_A1,2_VG1V_Vd0V_Id16uA	0.395367	0.249907	18.6322
R2282_A2,3_VG1V_Vd0V_Id7uA	0.0963595	0.949523	18.422
R2282_A3,1_VG1V_Vd0V_Id26uA	0.245538	0.496298	12.738
R2282_A3,4_VG1V_Vd0V_Id12uA	0.0113228	0.694832	16.9688
R2282_A4,1_VG1_Vd0V_Id31uA	0.239108	0.423771	12.2624
R2282_A5,1_VG1_Vd0V_Id16uA	0.298973	0.303025	18.2909

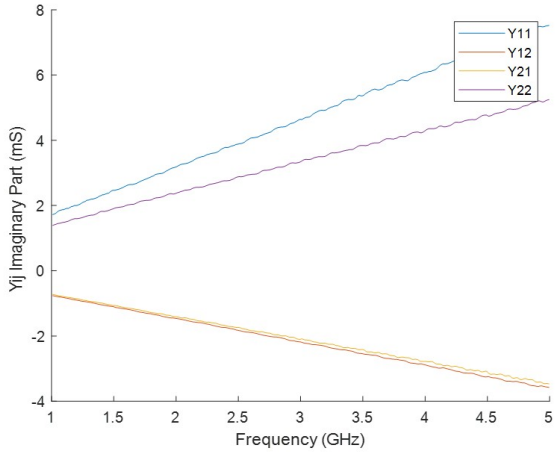
Table 3.2: Summary of extrinsic Inductances



((a)) Device R2282_A1,2_VG-7V_Vd0V_Id3nA



((b)) Device R2282_A2,3_VG-7_Vd0V_Id3nA



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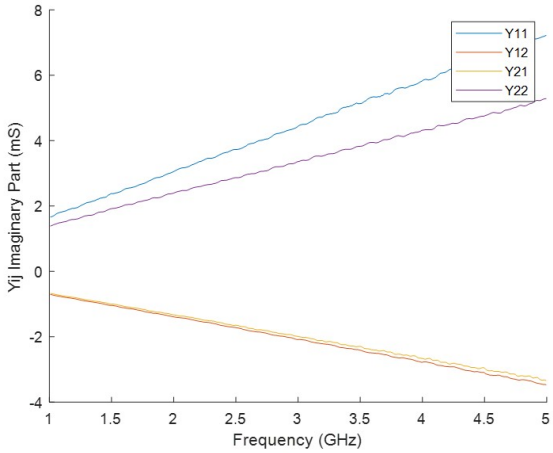
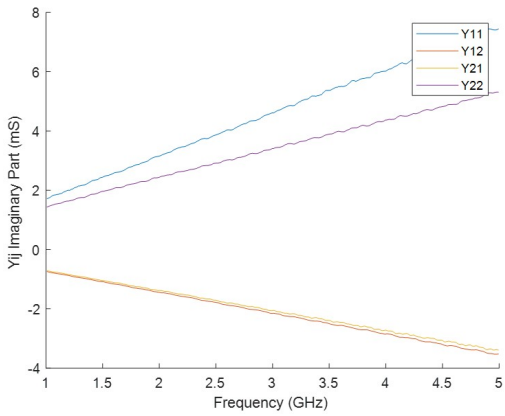


((d)) Device R2282_A3,4_VG-7V_Vd0V_Id4nA



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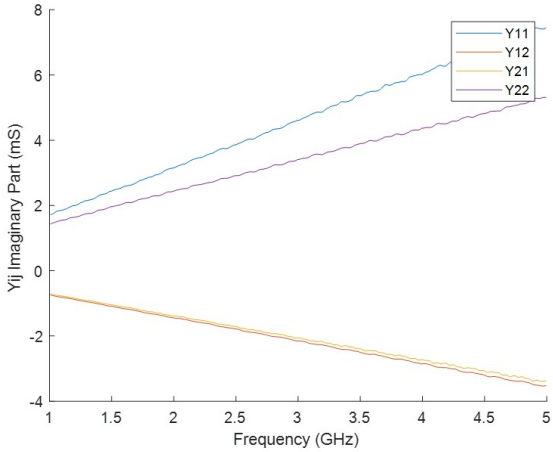

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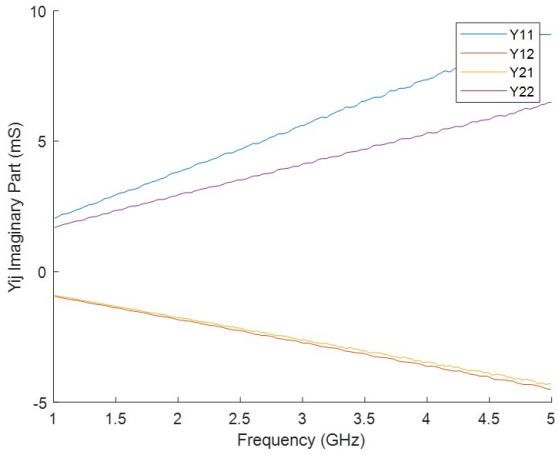

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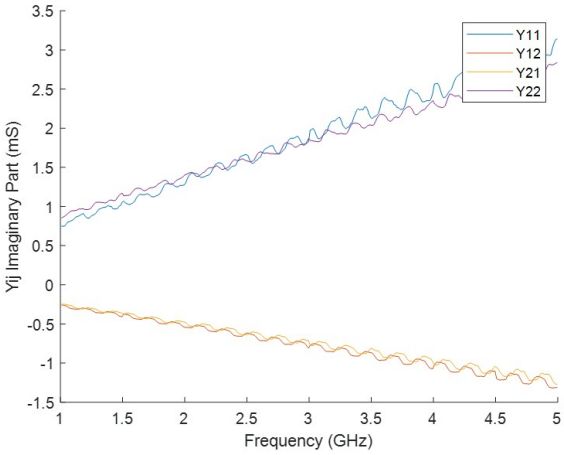
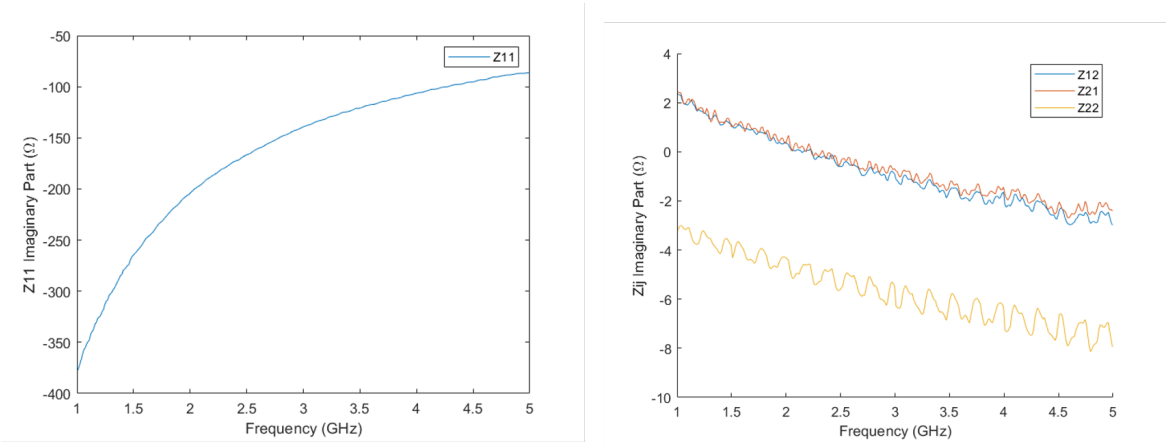


((d)) Device R2282_VG-7_Vd0V_Id140nA

Figure 3.1: Evolution of the Y parameters' imaginary part versus frequency, yielding the Cpg and Cpd pad capacitances



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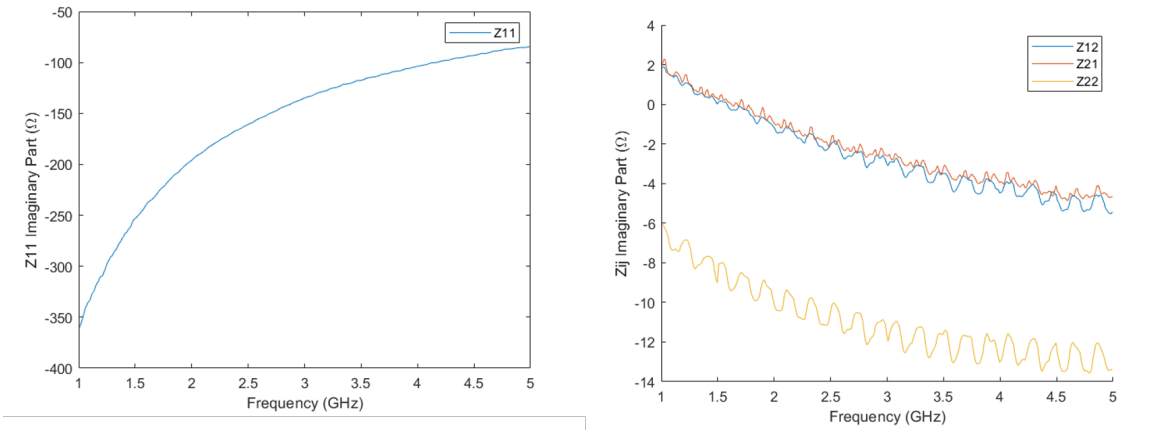
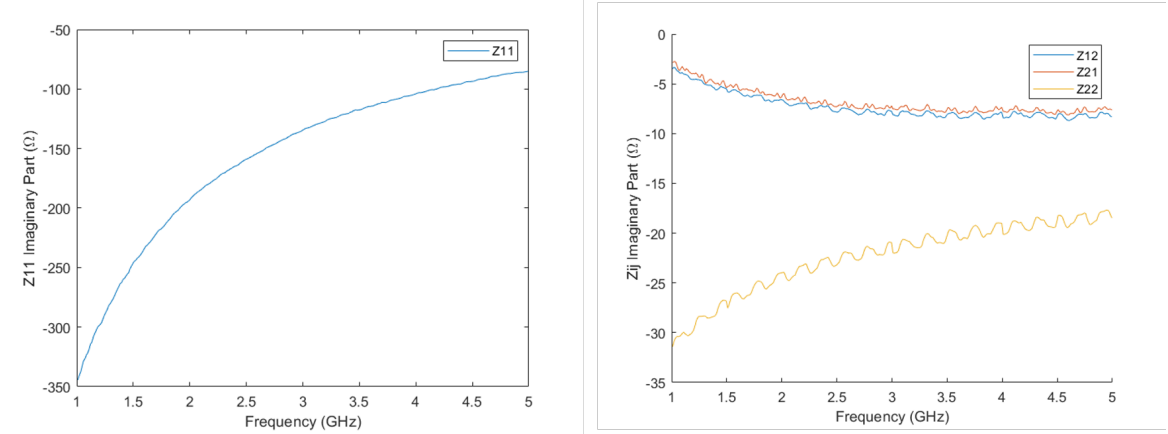
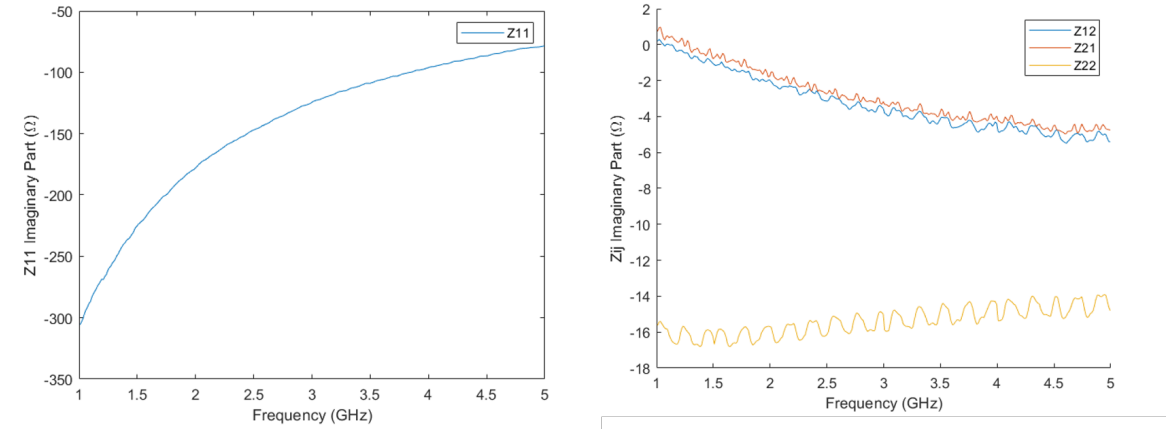


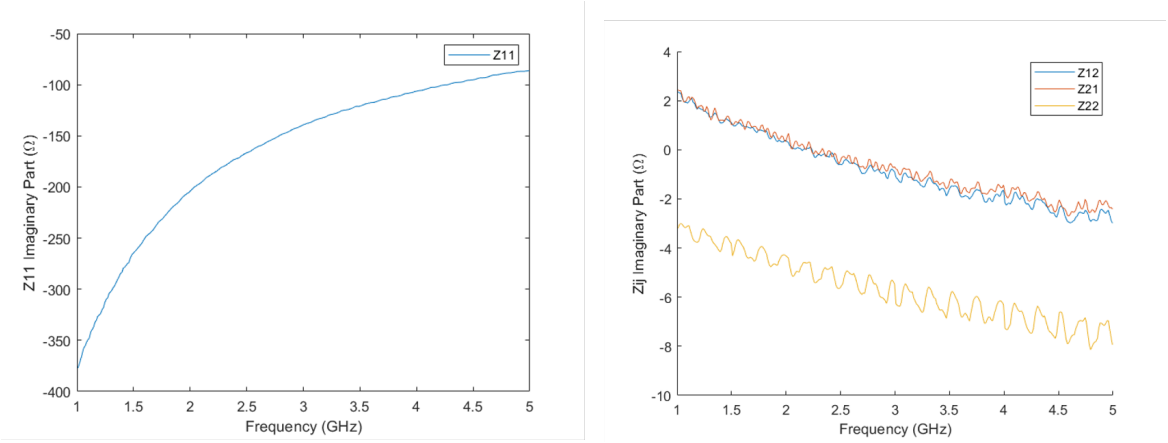
(b) Device R2282_A1,2_VG1V_Vd0V_Id16uA



(c) Device R2282_A2,3_VG1V_Vd0V_Id7uA.



(d) Device R2282_A3,1_VG1V_Vd0V_Id26uA



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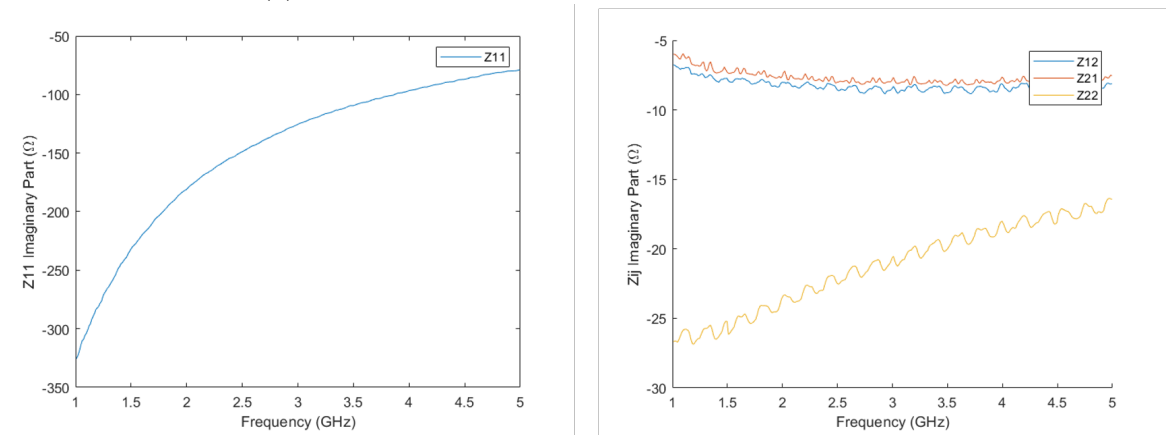
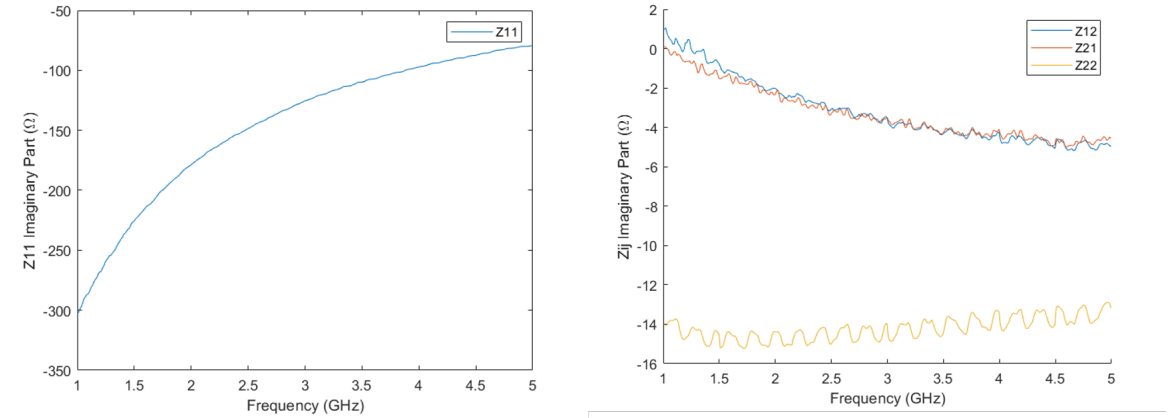


(f) Device R2282_A3,4_VG1V_Vd0V_Id12uA



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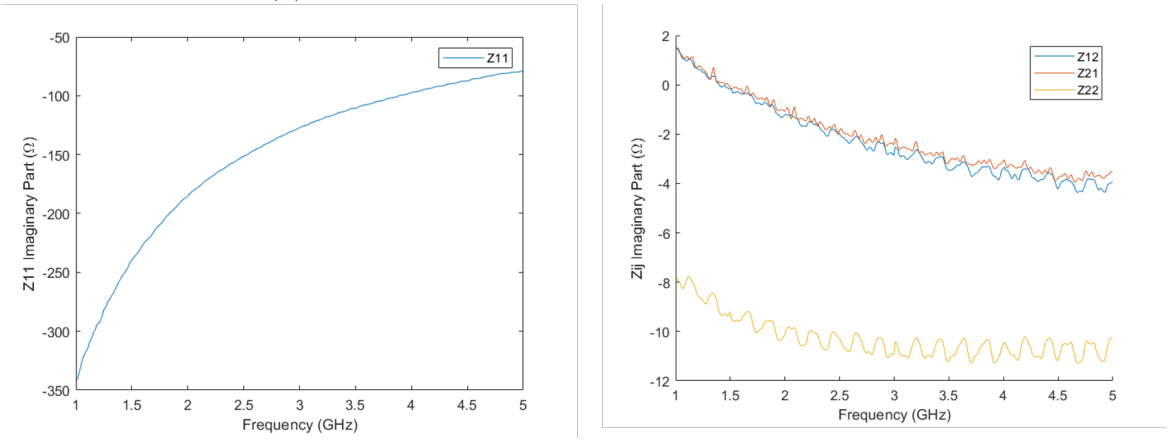

(h) Device R2282_A5,1_VG1_Vd0V_Id16uA

Figure 3.2: Evolution of the Z parameters' imaginary part versus frequency under forward gate bias voltage and zero drain bias voltage.

Conclusion

This project dealt with a method for determining the small-signal equivalent circuit components of FETs. This method consists in a direct determination of all the FET parasitic elements, including the C_{pg} and C_{pd} pad capacitances. The knowledge of these parasitic element values allows us to determine the intrinsic small-signal parameters after a few simple matrix manipulations. Compared with the conventional method, based on S parameters fit in a broad frequency range, the method implemented has several advantages:

1. All the extrinsic and intrinsic components are directly determined.
2. The method implemented is fast and accurate and only a network analyzer is needed.
3. The method is very well suited for wafer-probing systems since it is very fast and is performed in a low-frequency range.
4. The method is very well suited to obtain a large amount of data directly connected with the design or the process of FET's.

References

[1] R. G. Brady, C. H. Oxley and T. J. Brazil, "An Improved Small-Signal Parameter-Extraction Algorithm for GaN HEMT Devices," in IEEE Transactions on Microwave Theory and Techniques, vol. 56, no. 7, pp. 1535-1544, July 2008, doi: 10.1109/TMTT.2008.925212.

[2] G. Dambrine, A. Cappy, F. Heliodore and E. Playez, "A new method for determining the FET small-signal equivalent circuit," in IEEE Transactions on Microwave Theory and Techniques, vol. 36, no. 7, pp. 1151-1159, July 1988, doi: 10.1109/22.3650.

[3] F. Diamand and M. Laviron, "Measurement of the Extrinsic Series Elements of a Microwave Mesfet Under Zero Current Conditions," 1982 12th European Microwave Conference, Helsinki, Finland, 1982, pp. 451-456, doi: 10.1109/EUMA.1982.333103.

[4] K. W. Lee, "Corrections to "Source, drain, and gate series resistances and electron saturation velocity in ion-implanted GaAs FET's"," in IEEE Transactions on Electron Devices, vol. 33, no. 3, pp. 429-429, March 1986, doi: 10.1109/T-ED.1986.22506.

[5] J. Granlund, "Resistance associated with FET gate metallization," in IEEE Electron Device Letters, vol. 1, no. 8, pp. 151-153, Aug. 1980, doi: 10.1109/EDL.1980.25269.

[6] W. R. Curtice and R. L. Camisa, "Self-Consistent FET Models for Amplifier Design and Device Diagnostics," 1984 IEEE MTT-S International Microwave Symposium Digest, San Francisco, CA, USA, 1984, pp. 427-429, doi: 10.1109/MWSYM.1984.1131817.

[7] H. A. Willing, C. Rauscher and P. de Santis, "A Technique for Predicting Large Signal Performance of a GaAs MESFET," 1978 IEEE-MTT-S International Microwave Symposium Digest, Ottawa, ON, Canada, 1978, pp. 132-134, doi: 10.1109/MWSYM.1978.1123813.